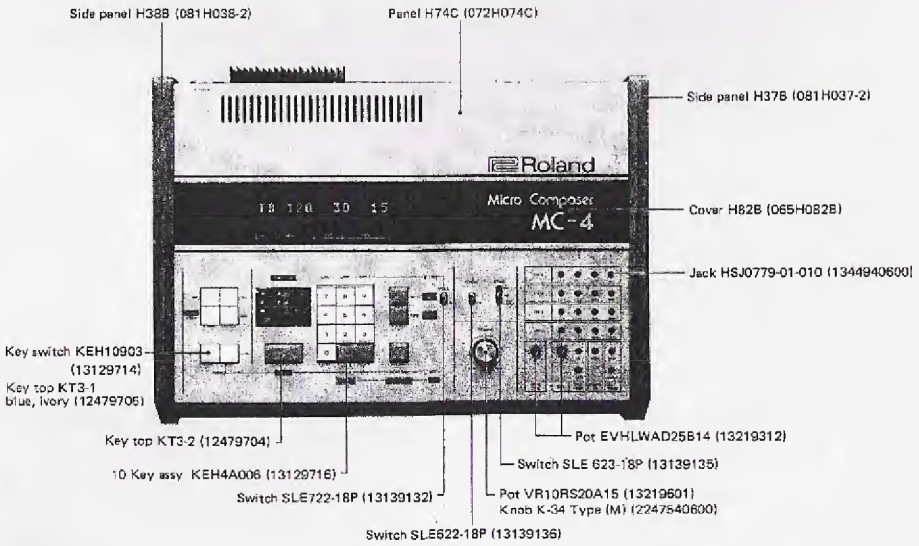
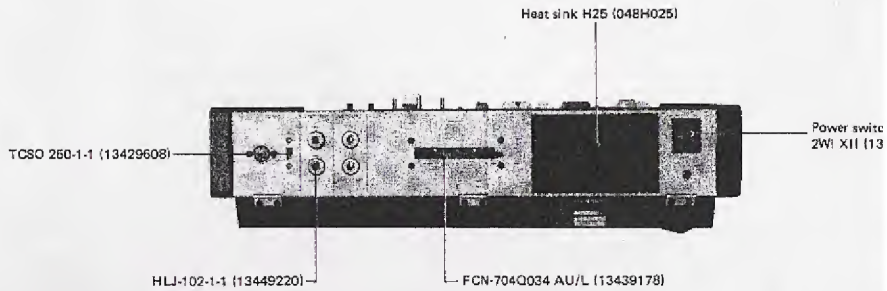
MC-4 SERVICE NOTES

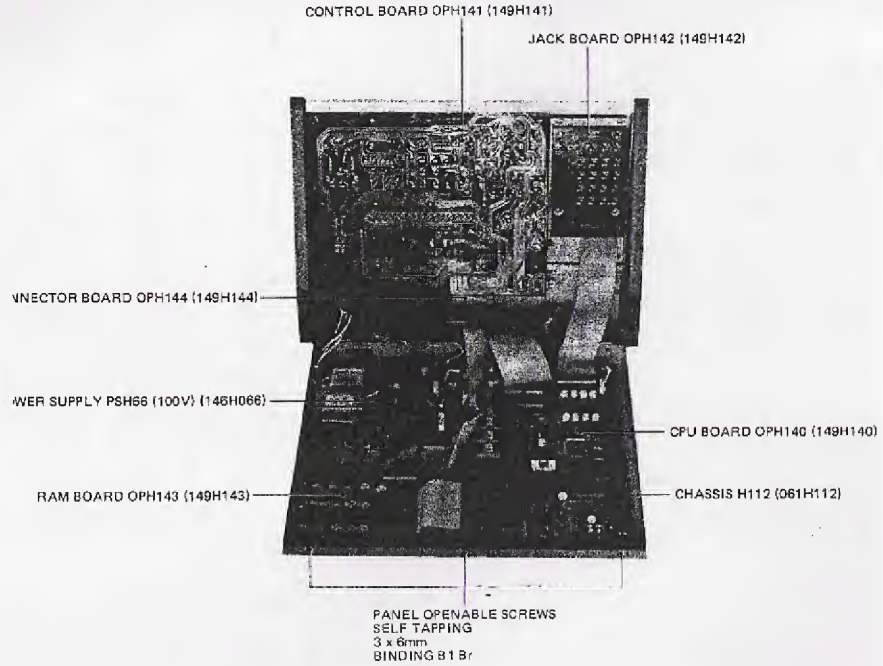
First Edition

SPECIFICATIONS

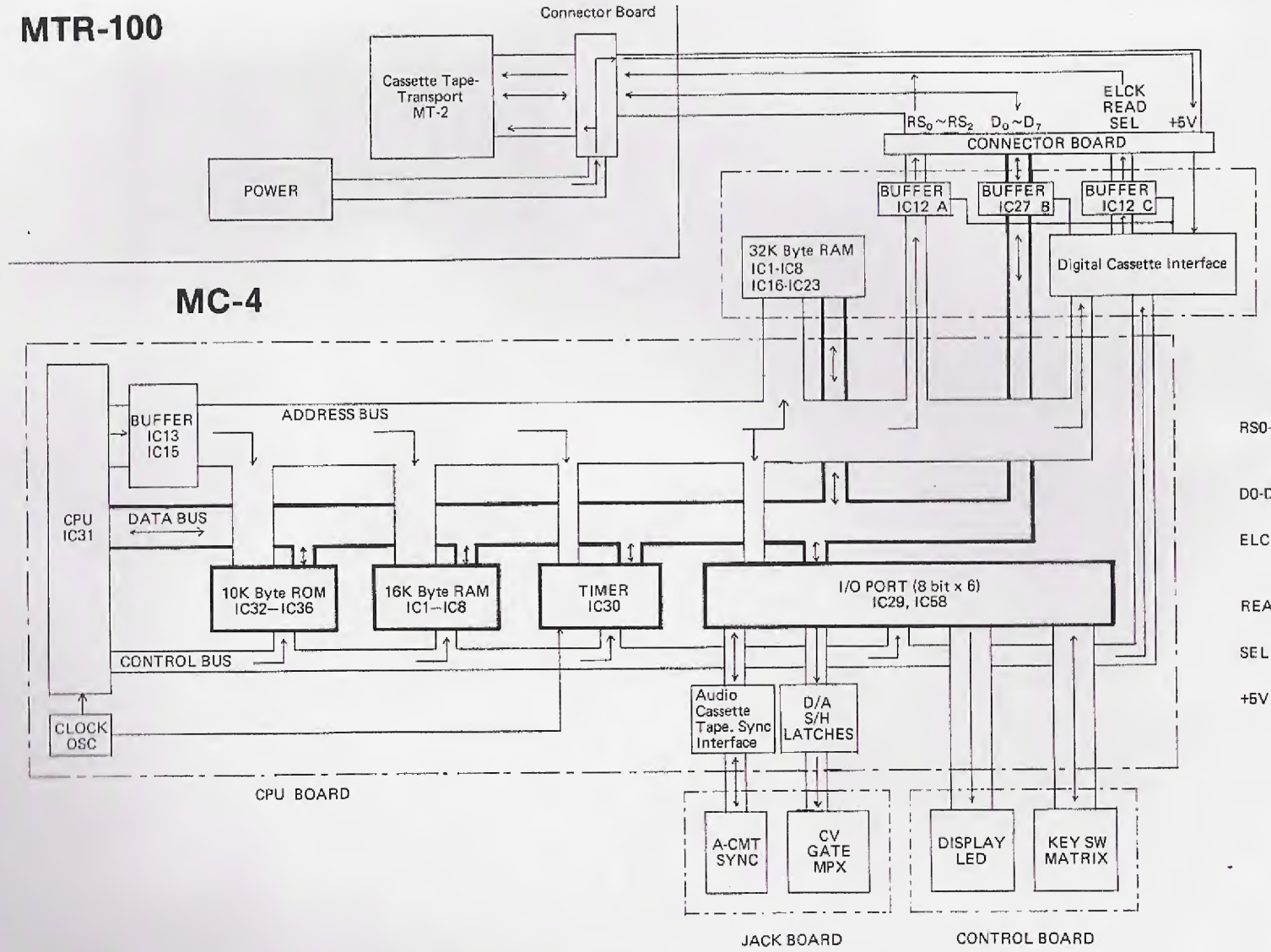
Memory Capacity	MC-4A [w/out OM-4] apx 3900 notes [16 K byte version] MC-4B [with OM-4] apx 12000 notes [48 K byte version]	
** OM-4:	optional memory board with interface for MTR-100	
Output	4 channels	each channel has:
	CV-1	[0V—10.42V, 125 steps, 83.3mV/step]
	CV-2	[0V—10.42V, 125 steps, 83.3mW/step]
	Gate	[off=0V, on=12V]
	MPX	[off=0V, on=12V]
Ext Input	CV	[0V—10.42V]
	Gate	[threshold +2.5V]
	Calibration Knob	
Tempo CV Input	CV	[0V—10.42V]
Ext Sync	Input	[threshold +2.5V]
	Output	[0—5V]
Total Tune Knob		[+/— 100 cents]
Tempo Knob		[—50% to +100%]
Shift Map	7: CV1+GATE	8: GATE REWRITE 9: TUNE
	4: CV2	5:MPX
	1: CV1	2: STEP TIME 3: GATE TIME
	0: Available Memory (%)	
Dimensions	471 x 348 x 124 mm	
Weight	6.1kg (MC-4A), 6.3kg (MC-4B)	
Power	30W	







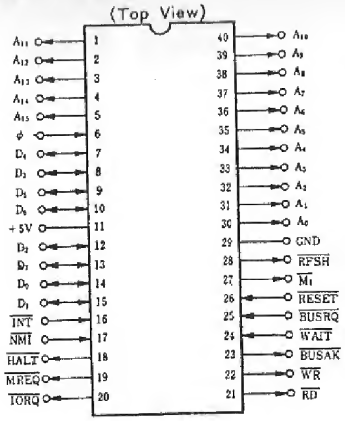
MTR-100



SIGNALS THROUGH RAM BOARD CONNECTORS

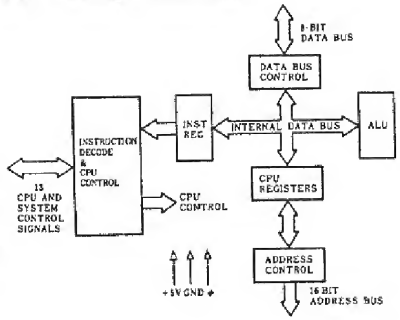
RS0-RS2	:	ADDRESSES A0-A2 Select one of MT-2 internal 8 registers.
D0-D7	:	PARALLEL BUS Transfers 8 bit data from/to MT-2.
ELCK	:	SYNC CLOCK derived from CPU CLOCK Controls MT-2 MT-2 operations.
READ	:	Signals MT-2 direction of data flow on the data buss.
SEL	:	Indicates that CPU names MT-2. Gates Buffers A, B and C.
+5V	:	Informs Interface that MT-2 power is ON.

JAN.13,1982



μPD780 C/D-1

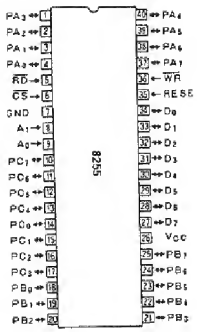
8 BIT MICROPROCESSOR



μPD8255C

PROGRAMMABLE PERIPHERAL INTERFACE

24 Programmable I/O Pins



BASIC OPERATION

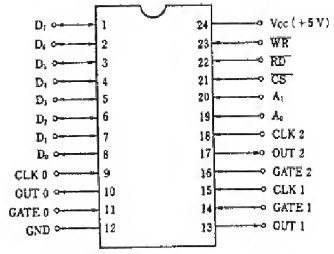
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A – DATA BUS
0	1	0	1	0	PORT B – DATA BUS
1	0	0	1	0	PORT C – DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS – PORT A
0	1	1	0	0	DATA BUS – PORT B
1	0	1	0	0	DATA BUS – PORT C
1	1	1	0	0	DATA BUS – CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS – 3-STATE
1	1	0	1	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS – 3-STATE

In the MC-4 8255C operates in MODE 0 and 8253 in different MODEs.

μPD8253C-5

PROGRAMMABLE INTERVAL TIMER

3 Independent 16-Bit Counters



$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation 3-State
1	X	X	X	X	Disable 3-State
0	1	1	X	X	No-Operation 3-State

ADDRESS BUS

A14, A15 Used to select the following memory blocks through respective Address Decoders.

Address Decoder	Memory	
IC60	IC32-IC36	ROMs on CPU Board
IC10, IC12	IC1-IC8,	RAMs on CPU Board
IC24, IC25	IC1-IC8, IC16-IC23	RAMs on RAM Board

A0-A7 Used to select I/O Devices through Port Address Decoder IC57 on CPU Board. (See I/O MAP right)

IC29 [70] D/A, MODE LED Display, DIN OUT, A/D IN, Clock Out, CYCLE SW IN

IC30 [40] Timing Signals generation, Total Time measurement

IC58 [60] Key Scanning, Dot Display, Metronome, Mode sw IN, DIN IN

I/O MAP

40	IC30 8253
50	EXT MTR-100
60	IC58 8255
70	IC29 8255

The numbers [40], [60] and [70] above, also shown in the CPU circuit diagram, are abbreviated I/O divice numbers in hex. to be represented on address bus, that is x x 4 x, x x 6 x and x x 7 x. If bits 0111 (7) appear on A7-A4, IC57 selects IC29. Then bits on A1-A0 will cause one of the following in IC29 to be selected; 00-Port A, 01-Port B, 10-Port C and 11-Control Word Register.
Similarly, if 0100 (4) are on A7-A4, IC57 selects IC30, and 00 on A1-A0 Counter Ø.

DATA BUS Used to transfer Instructions and Data to/from I/O Devices and RAMs.

Ø 4MHz, square Clock signal derived from devide-by-2 divider IC18

$\overline{MREQ}$ Indicates that the address bus holds a valid memory address for a memory read or memory write cycle.

$\overline{IORQ}$ Indicates that lower 8 bits (I/O Device Number) are on the address bus for an I/O read or I/O write cycle.

$\overline{RD}$ Indicates that the CPU wants to read data from memory or an I/O device.

$\overline{WR}$ Indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

$\overline{INT}$ Used as Tempo Clock in PLAY mode and is accepted by the CPU after it completes the current instruction being executed provided that CPU internal INT enable flip-flop is set on.

$\overline{NMI}$ Used to time the lightings of Dot Matrix Display and Shift LEDs, Key Switch Scanning, and the outputtings of CV and GATE. Accepted by the CPU unconditionally upon finishing of current instruction.

$\overline{WAIT}$ Used to keep the CPU wait for 1 clock cycle to provide enough performance time for relatively low speed ROM and RAM being accessed by the CPU.

$\overline{M1}$ Indicates Fetch cycle.

$\overline{RESET}$ Used to reset and start the CPU from a power down condition resulting from failure or initial start-up of the processor.

CIRCUIT DESCRIPTION

CPU BOARD

When CPU is initialized with power-on RESET signal, it wants to read operational program (software – instruction) stored at address $(0000)_{16}$ to starts controlling the MC-4.
With 0s on the address bus (A11-A15) and MREQ, ROM Address Decoder IC60 selects ROM [A] IC36 which in turn transfers data from accessed memory cells to D0-D7. CPU proceeds steps with fetched instruction.
The following is one of steps will be done.
(1) To transfer data to or from RAMs
(2) To transfer data to or from I/O ports or Programmable Timer

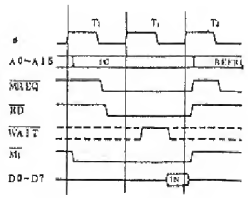


Fig. 1

ADDRESS MAP

0000	ROM [A] IC36
	ROM AREA
27FF	ROM [E] IC32
	BLANK
4000	IC1-IC8 (CPU BOARD)
	RAM AREA
8000	IC1-IC8 (RAM BOARD)
C000	IC16-IC23 (RAM BOARD)
FFFF	

(1) Accessing to RAMs IC1-IC8

The CPU places RAM address onto Address bus, then outputs necessary signals as shown in Fig. 2.

Eight 16K x 1 bit RAMs are connected in parallel to form a 16K x 8 bit RAM block. The 14 address bits required to decode 1 of the 16,384 cell locations within MSK4116 are multiplexed onto 7 address inputs (A0-A6) of RAMs. First, lower order 7 bits are fed to RAMs through RAM Address Multiplexers (IC9 and IC11) and latched into the RAMs' on-chip address latches by $\overline{RAS}$. Second, higher order 7 bits are fed to the RAMs when SEL pins of IC9 and IC11 go low by the delayed $\overline{MREQ}$ coming through pin 8 of IC12. These 7 bits are latched into RAMs' chips with $\overline{CAS}$ fed via RAM Address Decoders (IC10 and IC12), and an access to RAMs completes. Data are stored into selected cells by a combination of WRITE and $\overline{CAS}$, or retrieved from the memories in a read cycle in which $\overline{CAS}$ is active low.

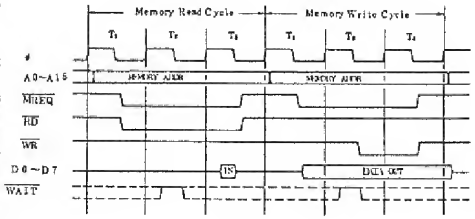


Fig. 2

(2) Accessing to Timer IC30 or I/O Ports IC29 and IC58

The CPU places port address (lower order 8 bits, A0-A7) onto the address bus, then outputs $\overline{IORQ}$, etc. as shown in Fig. 3.
As previously explained in CPU terminal functions "ADDRESS BUS", Port Address Decoder (IC57) selects the device which in turn reads or writes data.

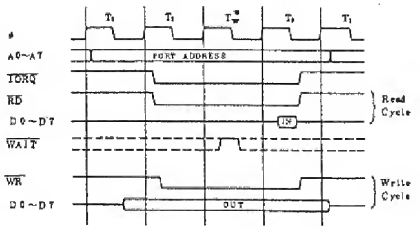


Fig. 3

D/A CONVERTER

The digital outputs from the PORT A of INTERFACE (IC29) are level-shifted by the transistors (TR5-TR11), pass through the CMOS INVERTERS (IC27, IC28), and undergo addition by the weighing resistors to become an analog voltage. Since the MC-4 has eight CVs, eight data are sampled in the time sharing system by the 4051 DMPX (IC46), held by the 081 (IC47-IC54) and output to the output jacks.
The resolution of the D/A converter is 1/12V, which corresponds to a half-tone step voltage.
The resistance error at the most significant bit, which affects the output error most significantly, is corrected by adjusting the VR3.
The VR2, equivalent to the width control of a synthesizer, should be adjusted so that the output changes in 1/12V step. The VR4 is used for offset adjustment of IC25.
For the GATEs (GT1-GT4) and MPXs (MPX1-MPX4), digital data are sampled by IC43 in the time sharing system (see Fig. 4).

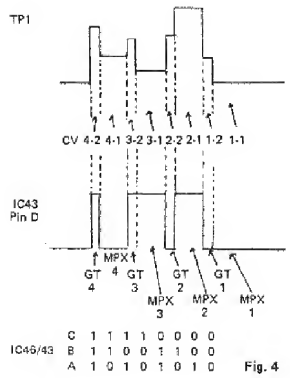


Fig. 4

CMT BLOCK

This block is composed of the input/output circuits for CMT DATA and TAPE SYNC CLOCK. The selection of CMT mode (CMT DATA) and PLAY mode (TAPE SYNC) is done by the hardware (IC41).
The output section delivers an approximately 2.1KHz signal when the DIGITAL DATA is H and an approximately 1.3KHz signal when the data is L (see Fig. 5).

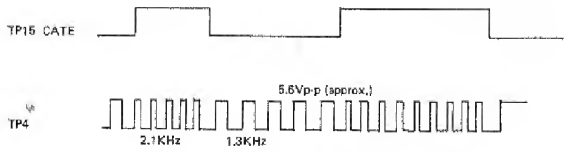


Fig. 5

For frequency modulation, IC42 is wired as a function generator whose frequency shifts to the other as R121 is connected to disconnected from charging/discharging time constant by FET SW (TR15).
The zener diodes (D11, D12) are used to prevent the output of the comparator OP amp (operating on +12V and −15V) from becoming unbalanced and to keep the duty ratio of the oscillation square wave-form to 50%. At the input section, a signal from the CMT/SYNC IN passes through a passive band-pass filter and is amplified by the OP amp (IC23). The signal further passes through a diode limitter, is amplified by IC22 and is separated into a signal for control and a signal for demodulation. The signal for demodulation is demodulated by the PLL (IC19) and the comparator (IC20) and is read via the 8255 INTERFACE (IC58).
The signal for control passes through a rectification circuit and is applied to the transistor switches (TR2, TR3) to set TP3 in active state. (While the CMT or SYNC signal is not inputted, TP3 is fixed at L level.) (See Fig. 6.)

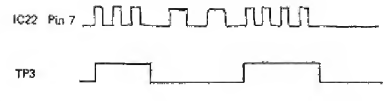


Fig. 6

CONTROL BOARD

DOT DISPLAY, SHIFT LEDs, KEY SWITCHES

These circuits are configured in separate matrices in a conventional fashion but one dimension of these share the same output pins of an address decoder IC1.
The address decoders (IC1 and IC2 in combination) places an L at output pins in sequence in symathy with NM1 clock brought into the pin of CPU as shown in Fig. 7. The following description will explicate Dot Display only since Shift LEDs- and KEY- scanning are self explanative.

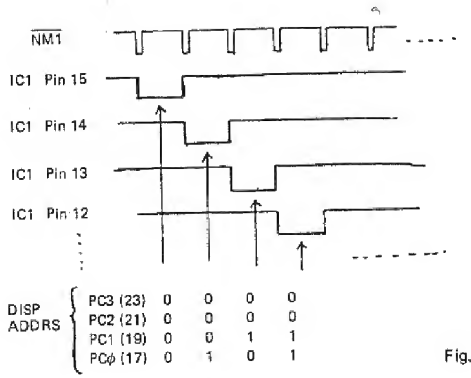


Fig. 7

DOT DISPLAY

Character signal consisting of 5 x 7 dots from the Dot Matrix Decoder IC9 is applied to fluorescent lamp indicator 16-MD-02Z in which the same dots in the individual digits are connected in parallel and led out as a common terminal, and the digit electrodes have individual leads (G1-G15) for external connection.
Although the same dot signals are fed to all digits simaltenously, only one digit whose grid is now H is allowed to illuminate – called dynamic lighting. But for human eyes those flickers are not perceptible.
Since filament laid across the tube serves as a common cathode for all digits, DC heating will cause brightness imbalance among digits due to potential variations between electrodes and the chathode.

METRONOME

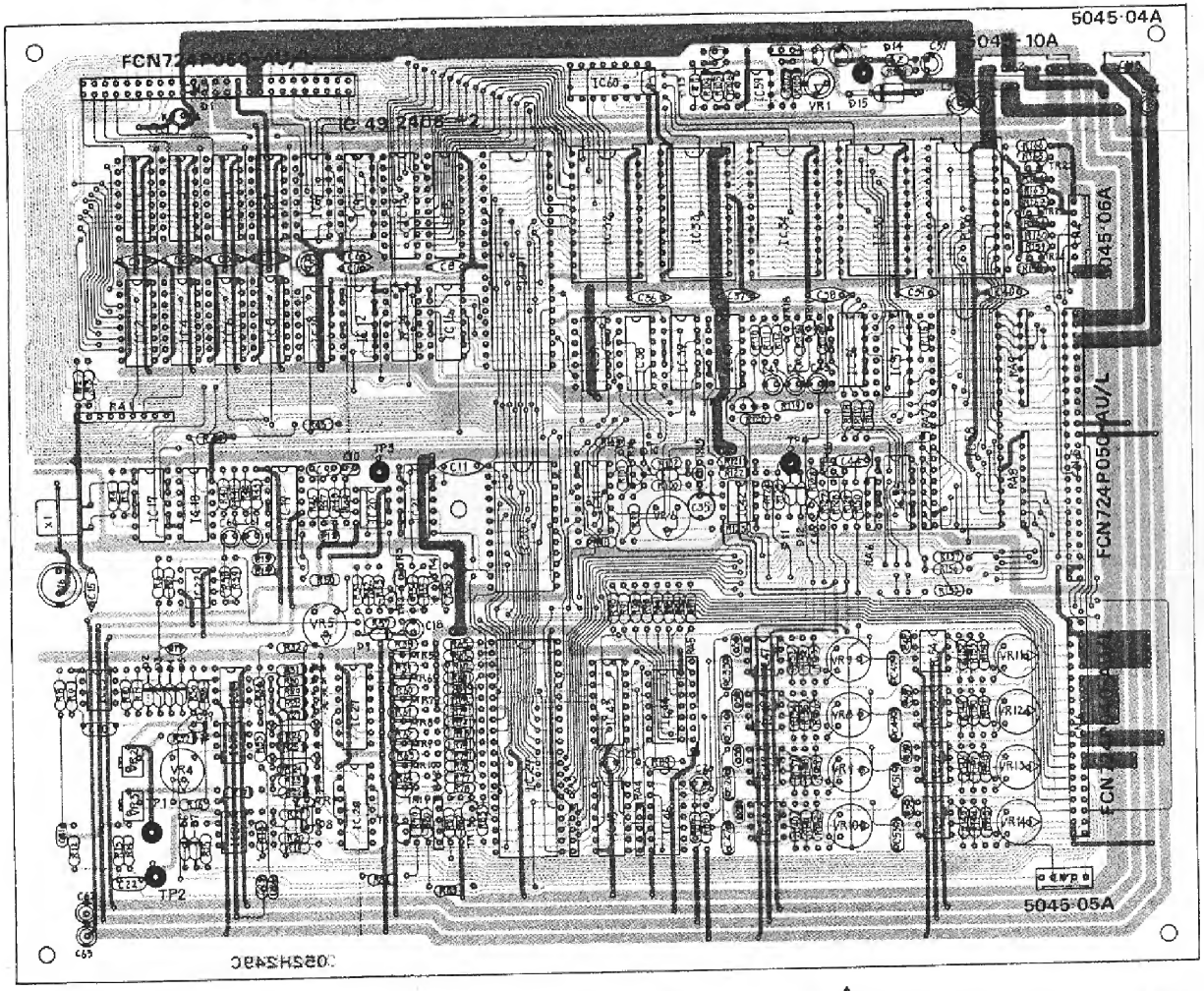
Output from oscillator IC7 is shaped into metronome-lick sound with percussive envelope developed in Tr35, C5 and R116 circuit.

TEMPO CLOCK GENERATOR

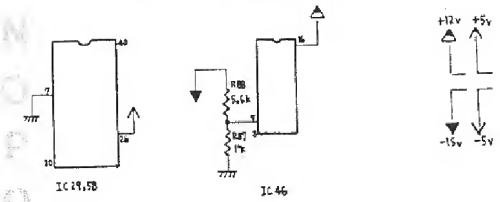
When nothing is connected to the TEMPO CV jack, a constant DC voltage of approximately 4.17V is applied to pin 5 of IC6 when the TEMPO control is set at the center. The voltage is applied to the VCO through IC6 and IC5, and the VCO oscillates at approximately 100KHz. Since the VCO's oscillation frequency changes linearly to the input voltage, when the input voltage is doubled, the oscillation frequency is also doubled. When the linearity is improper (especially at the high frequency range), the slew rate of IC3 is slow or TR31 is defective in most cases.
When an external CV is applied to the TEMPO CV IN jack, the TEMPO CLOCK is subjected to frequency modulation.

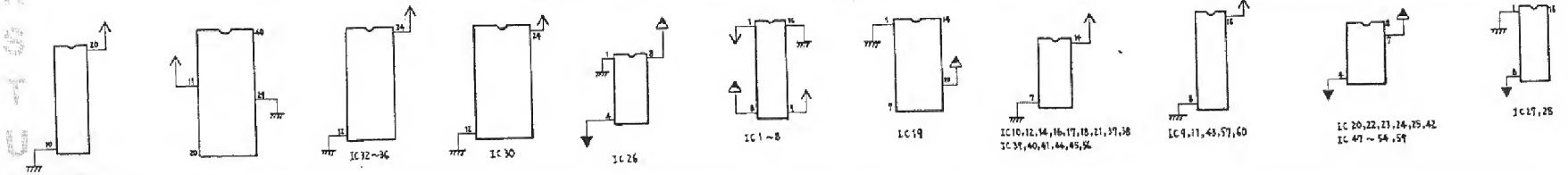
CPU BOARD OPH140(149H140)(pcb 052H249C)

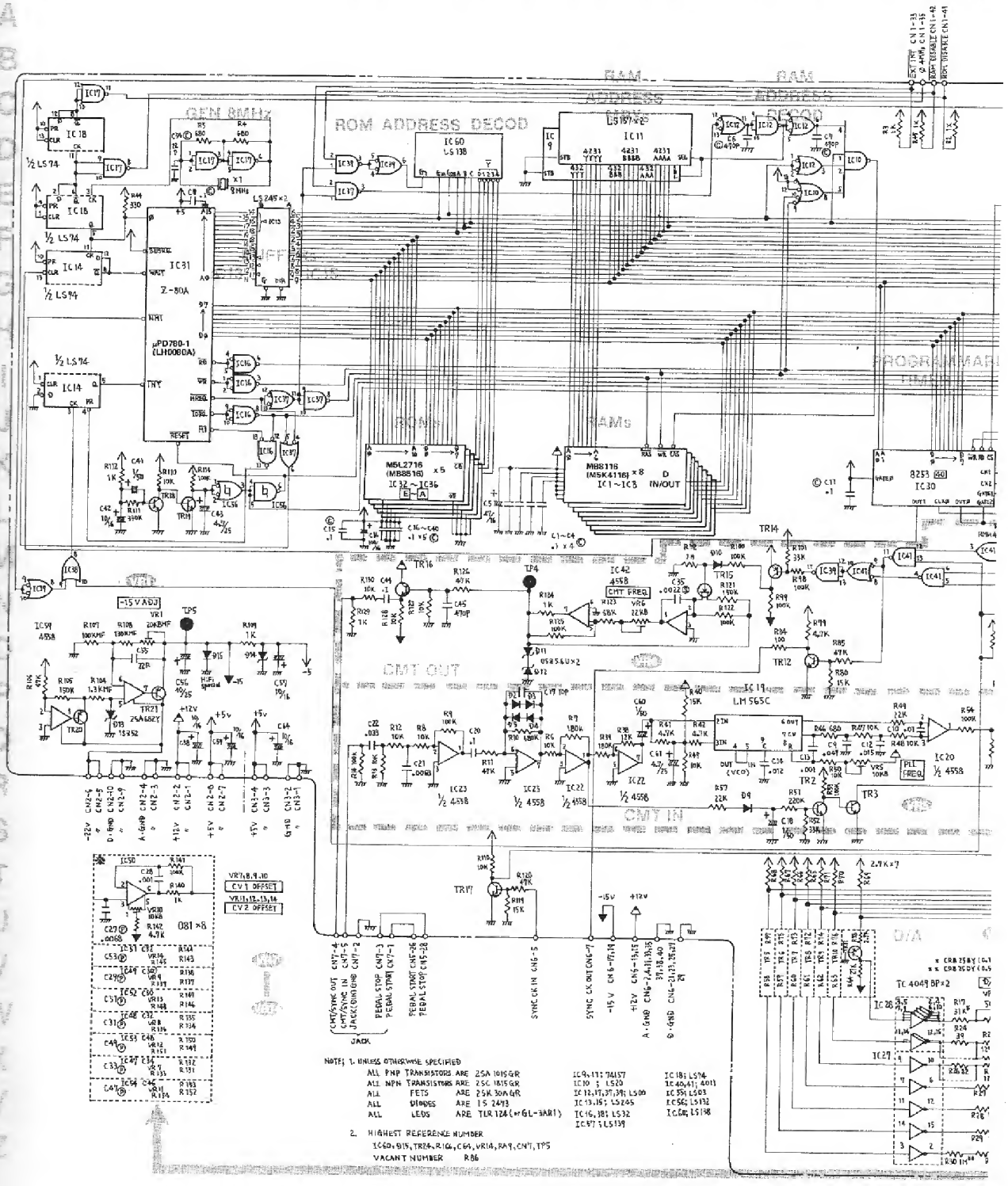
DZ Metal film CRB25DZ (0.5% 25PPM)
Carbon R-25J
Metal film CRB25FX (1% 100PPM)
Metal film CRB25DY (0.5% 50PPM)
Metal film CRB25BY (0.1% 50PPM)
Trimmer SR-19R
Metal film trimmer RJ-6P
Mylar (10%)
Polypropylene (5%)
Ceramic
2SC1815-GR
2SA1015-GR
2SK30A-GR
Resistor array
Pin 1
Metal film trimmer RJ-6S
1S2473
Zenner
LED TLR124 (or GL-3AR1)
2SA682Y
Test point LC-2-S
Jumper



SUPPLY VOLTAGES PIN CONNECTIONS (Top view)







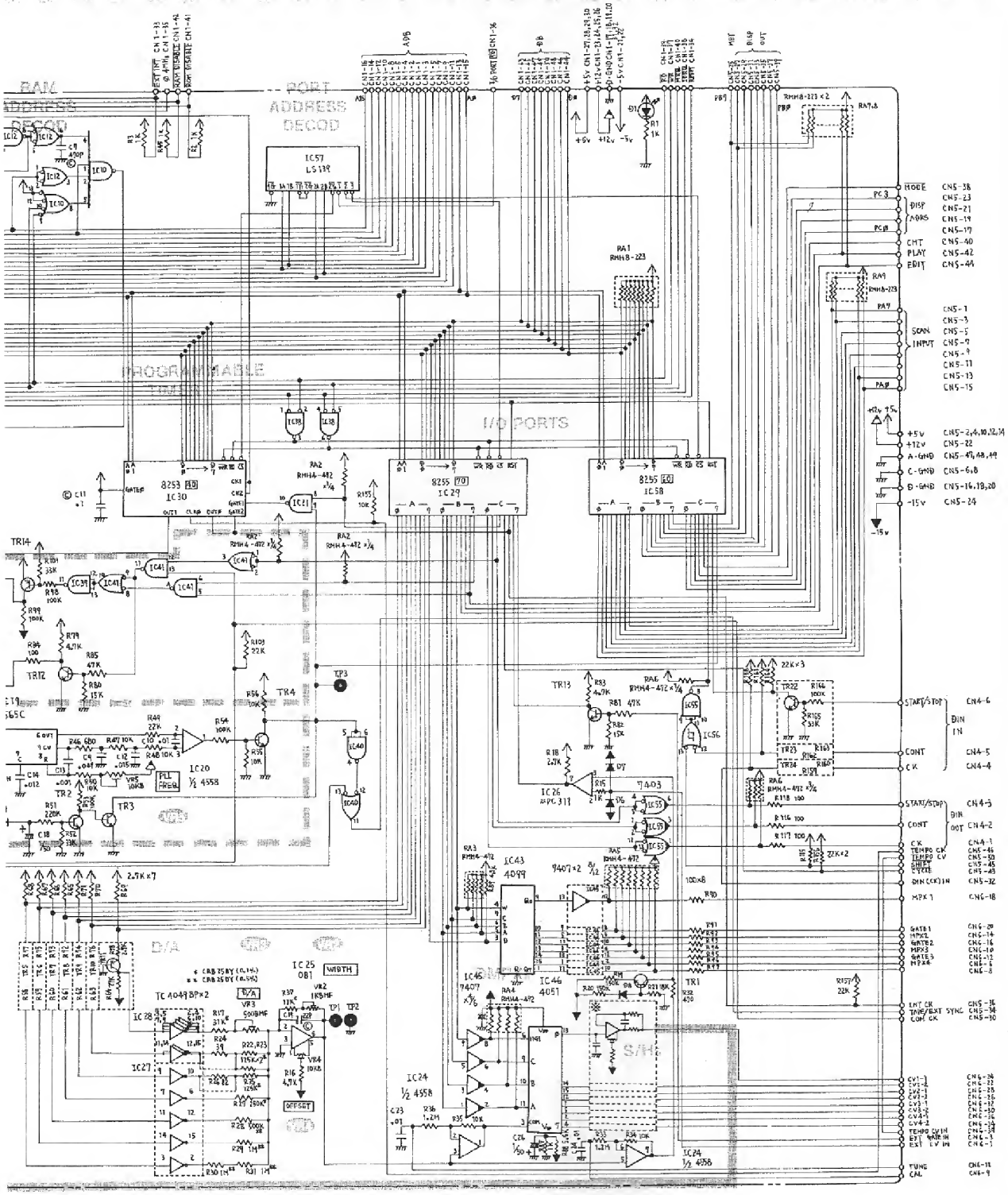
NOTE: 1. UNLESS OTHERWISE SPECIFIED

ALL PNP TRANSISTORS	ARE	2SA1015GR
ALL NPN TRANSISTORS	ARE	2SC1815GR
ALL FETS	ARE	2SK30AGR
ALL DIODES	ARE	1S2473
ALL LEDS	ARE	TLR124(or GL-3AR1)

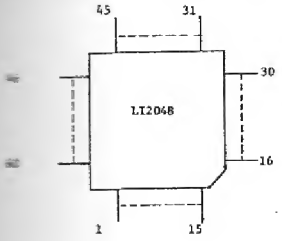
IC9,11; 74LS37
IC10 ; LS20
IC12,17,37,38; LS00
IC13,15; LS245
IC16,18; LS32
IC57 ; LS139

IC18; LS74
IC40,41; 4011
IC55; LS03
IC56; LS132
IC58; LS138

2. HIGHEST REFERENCE NUMBER
IC60; D15, TR24, R106, C64, VR14, RA9, CNT, TP5
VACANT NUMBER R86


RAM ADDRESS DECOD
PORT ADDRESS DECOD
PROGRAMMABLE TIMER
I/O PORTS
8253 PIO IC30
8255 PIO IC29
8255 PIO IC58
D/A
S/H
MODE
DISP
MORS
CMT
PLAY
EDIT
SCAN INPUT
+5V
+12V
A-GND
C-GND
B-GND
-15V
START/STOP
CONT
CK
TEMPO CK
TEMPO CV
GATE
STEP
DIN (CK) IN
MPX 1
ENT CK
TUNE
CAL

IC9
5 x 7 DOT MATRIX DECODER
LI-2048 (Top View)
(Surface mounted at foil side)



Pin Table

Pin No.	Signal	I/O	Description	Pin No.	Signal	I/O	Description
1	NC			31	D_{32}	O	Dot display output
2	NC			32	D_{34}	O	"
3	NC			33	D_{35}	O	"
4	D_{63}	O	Dot display output	34	D_{01}	O	Dot display/print output
5	D_{64}	O	"	35	D_{02}	O	Dot display output
6	D_{63}	O	"	36	D_{03}	O	"
7	V_{DD}			37	D_{04}	O	"
8	GND			38	GND		
9	D_{62}	O	Dot display output	39	D_{05}	O	Dot display output
10	D_{61}	O	Dot display/print output	40	A_0	I	Dot select input
11	D_{55}	O	Dot display output	41	A_1	I	"
12	D_{54}	O	"	42	A_2	I	"
13	D_{53}	O	"	43	A_3	I	"
14	D_{52}	O	"	44	A_4	I	"
15	D_{51}	O	Dot display/print output	45	A_5	I	"
16	NC			46	NC		
17	NC			47	A_6	I	Dot select input
18	D_{11}	O	Dot display/print output	48	A_7	I	"
19	D_{12}	O	Dot display output	49	A_8	I	"
20	D_{13}	O	"	50	A_9	I	"
21	D_{14}	O	"	51	CE_1	I	Chip enable input
22	D_{15}	O	"	52	CE_2	I	Display/print select input
23	D_{21}	O	Dot display/print output	53	V_N		
24	D_{22}	O	Dot display output	54	D_{75}	O	Dot display output
25	D_{23}	O	Dot display output	55	D_{76}	O	Dot display output
26	D_{24}	O	"	56	D_{73}	O	"
27	D_{25}	O	"	57	D_{72}	O	"
28	D_{31}	O	Dot display/print output	58	D_{71}	O	Dot display/print output
29	NC			59	NC		
30	D_{32}	O	Dot display output	60	NC		

CPU BOARD CN5		CONTROL BOARD CN1
PA7		+5V
PA6		+5V
PA5	SCAN IN	C·GND
PA4		C·GND
PA3		+5V
PA2		+5V
PA1		+5V
PAØ		D·GND
PCØ	DISP ADRS	D·GND
PC1		D·GND
PC2		+12V
PC3		-15V
PB7		PEDAL·START
PB6		PEDAL·STOP
PB5		COM·CK
PB4	DISP OUT	DIN·CK·IN
PB3		TAPE/EXT SYNC
PB2		INT·CK
PB1		MODE
PBØ		CMT
NC		PLAY
CYCLE		EDIT
SHIFT		TEMPO·CK
A·GND		A·GND
A·GND		TEMPO·CV

CPU BOARD CN1		RAM BOARD CN2
A7		A8
A6		A9
A5		A10
A4		A11
A3		A12
A2		A13
A1		A14
A0		A15
D·GND		D·GND
D·GND		D·GND
-5V		-5V
+12V		+12V
+12V		+12V
+5V		+5V
+5V		+5V
D·GND		D·GND
EXT·INT		RESET
Ø 4MHz		5/6 PORT
WR		IORQ
RD		MRQ
ROM·DIS		RAM·DISABLE
D7		D0
D6		D1
D5		D2
D4		D3

WIRING DATA TABLE

CPU BOARD CN7		JACK
1	PEDAL START	
2	JACK(DIN) GND	
3	PEDAL STOP	
4	CMT/SYNC OUT	
5	CMT/SYNC IN	

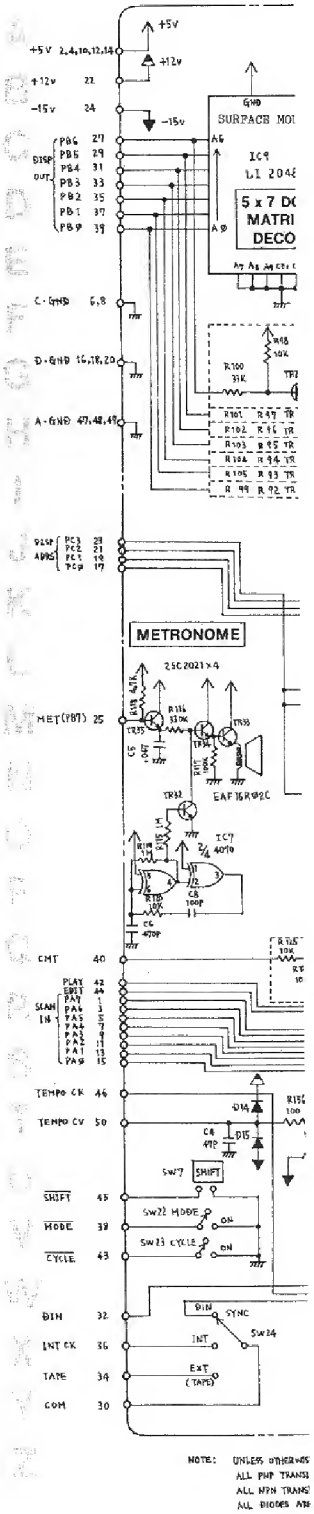
CPU BOARD POWER CN3		SUPPLY
1	GND	
2	GND	
3	+5V	
4	+5V	

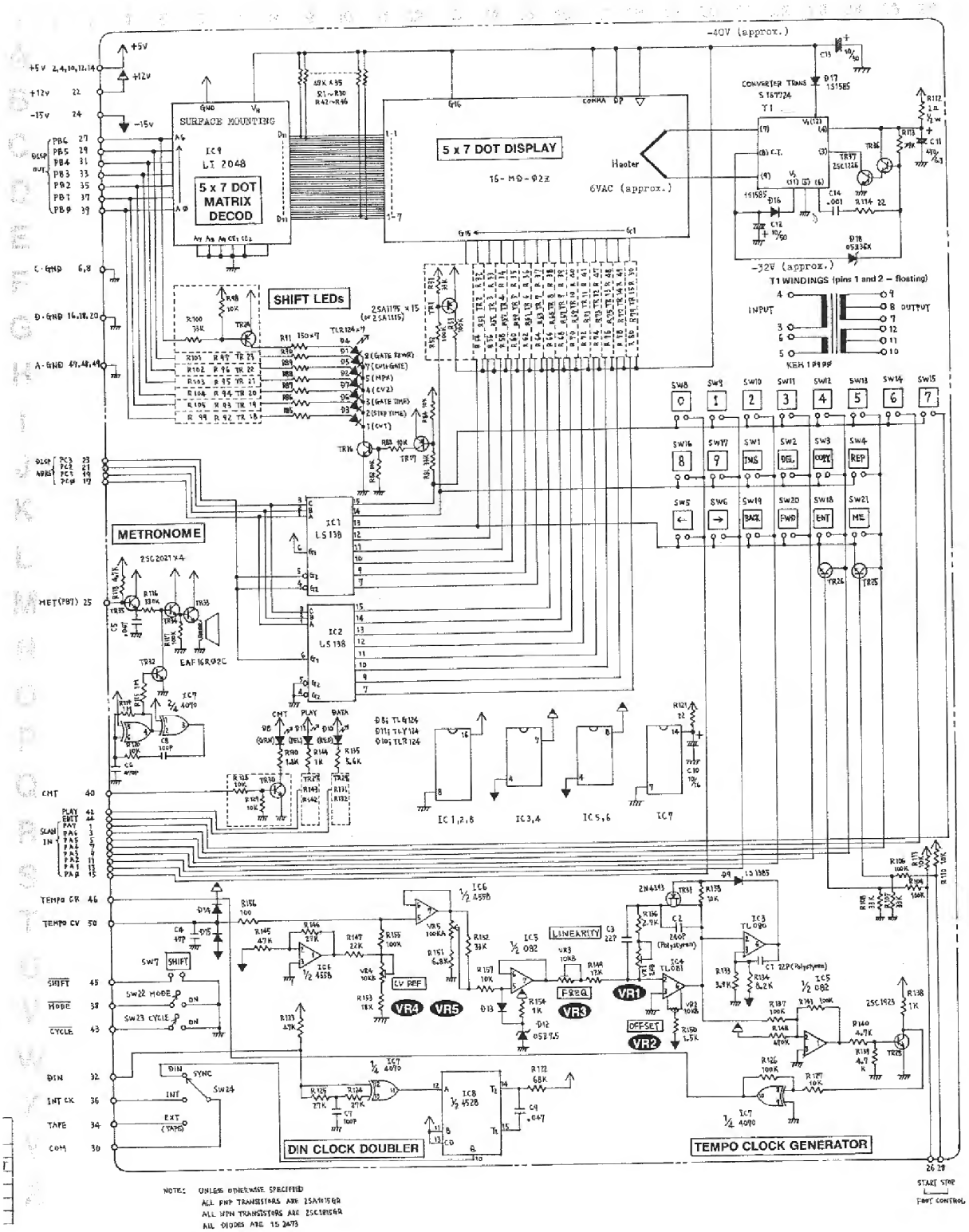
CPU BOARD CN6		Jack BOARD CN1
1	EXT·CV·IN	2 A·GND
3	EXT·GATE·IN	4 A·GND
5	SYNC·CK·IN	6 MPX4
7	SYNC·CK·OUT	8 GATE 4
9	CAL	10 MPX3
11	TUNE	12 GATE 3
13	+12V	14 MPX2
15	+12V	16 GATE 2
17	-15V	18 MPX1
19	-15V	20 GATE1
21	D GND	22 CV 1-2
23	D·GND	24 1-1
25	D·GND	26 2-2
27	D GND	28 2-1
29	D·GND	30 3-2
31	A·GND	32 3-1
33	A·GND	34 4-2
35	A·GND	36 4-1
37	A GND	38 A·GND
39	TEMPO·CV·IN	40 A·GND

(RAM BOARD) CN1		OUT PUT BUS
1	ELCK	2 GND
3	READ	4
5	D7	6
7	D6	8
9	D5	10
11	D4	12
13	D3	14
15	D2	16
17	D1	18
19	DØ	20
21	SEL	22
23	RS2	24
25	RS1	26
27	RSØ	28
29	+5V	30
31	—	32 —
33	—	34 —

CPU BOARD CN2		POWER SUPPLY
1	+12V	
2	+12V	
3	A·GND	
4	A GND	
5	-22V	
6	-22V	
7	+5V	
8	+5V	
9	D·GND	
10	D GND	

CPU BOARD CN4		DIN
1	CK	
2	CONT	DIN OUT
3	START/STOP	
4	CK	
5	CONT	DIN IN
6	START/STOP	





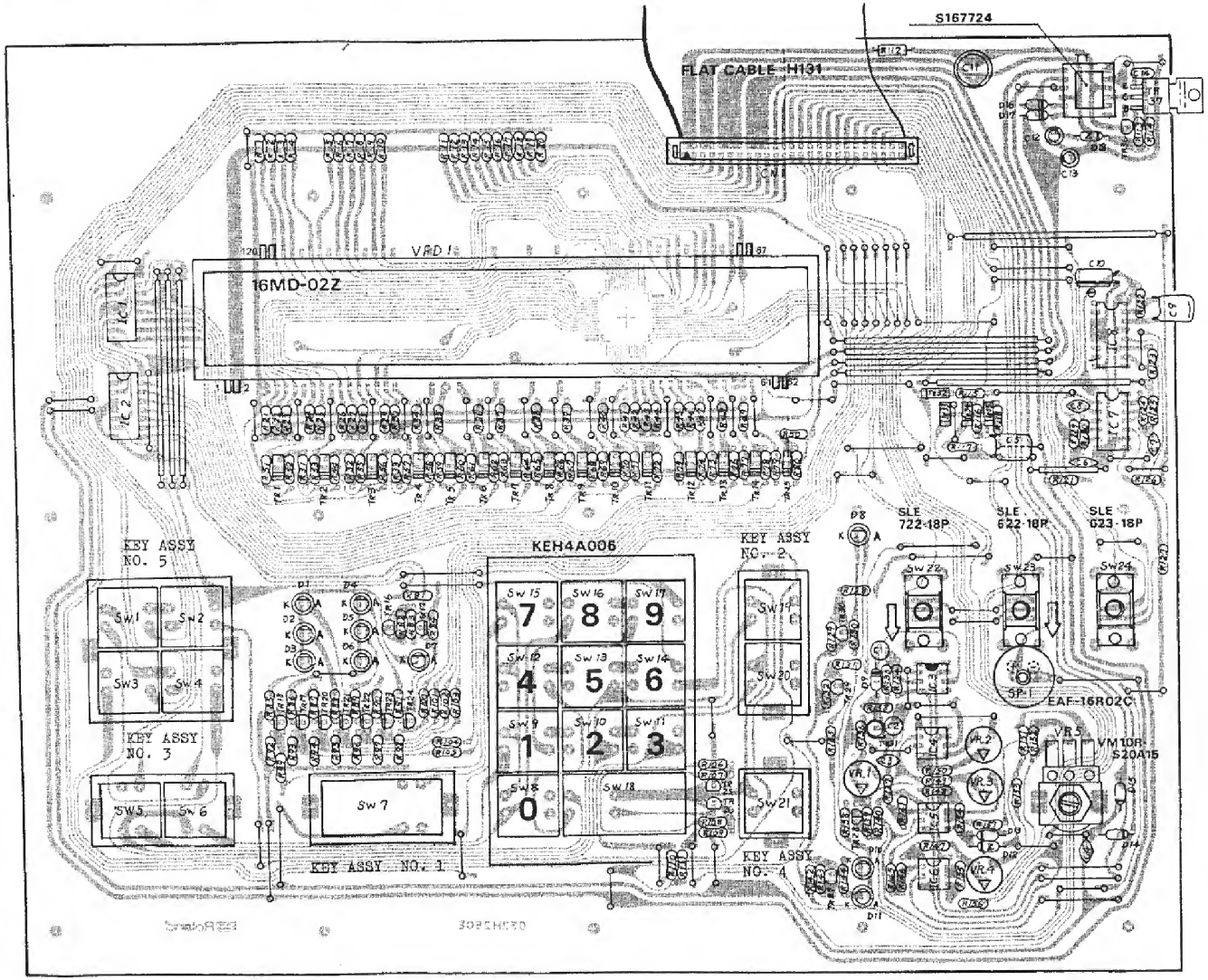
NOTE: UNLESS OTHERWISE SPECIFIED
ALL PNP TRANSISTORS ARE 2SA1015GR
ALL NPN TRANSISTORS ARE 2SC1815GR
ALL DIODES ARE 1S 2473

16MD-02Z

PIN CONNECTION (TOP VIEW)

124	123	122	121	120	119	118	117	116	115	114	113	112	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64	63
NP	NP	NP	NP	G16	1-1	2-1	3-1	G15	4-1	5-1	G14	1-2	2-2	3-2	G13	4-2	5-2	G12	NP	NP	NP	G11	NP	NP	G10	NP	NP	NP	G9	NP	NP	NP	G8	NP	NP	G7	NP	NP	NP	G6	NP	NP	G5	1-3	2-3	3-3	G4	4-3	5-3	G3	1-4	2-4	3-4	G2	4-4	5-4	G1	NP	NP	NP	NP

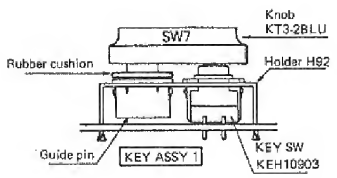
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62
F	F	NP	NP	G16	1-5	2-5	3-5	G15	4-5	5-5	G14	1-6	2-6	3-6	G13	4-6	5-6	G12	NP	NP	NP	G11	NP	NP	G10	NP	NP	NP	G9	NP	NP	NP	G8	NP	NP	G7	NP	NP	NP	G6	NP	NP	G5	1-7	2-7	3-7	G4	4-7	5-7	G3	NP	NP	▽	G2	com	DP	G1	NP	NP	F	F

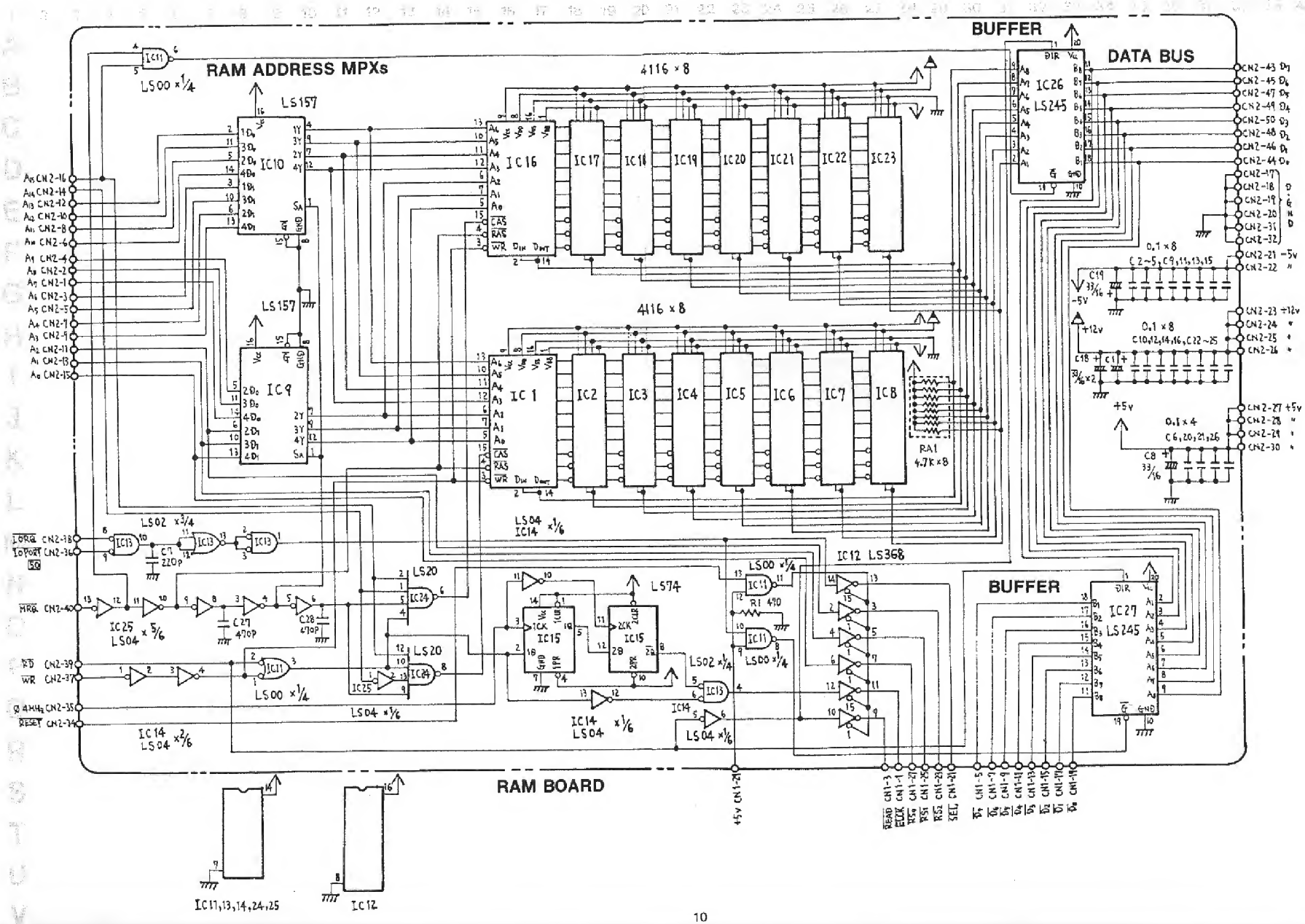


CONTROL BOARD
OPH141(149H141)
(pcb 052H250E)

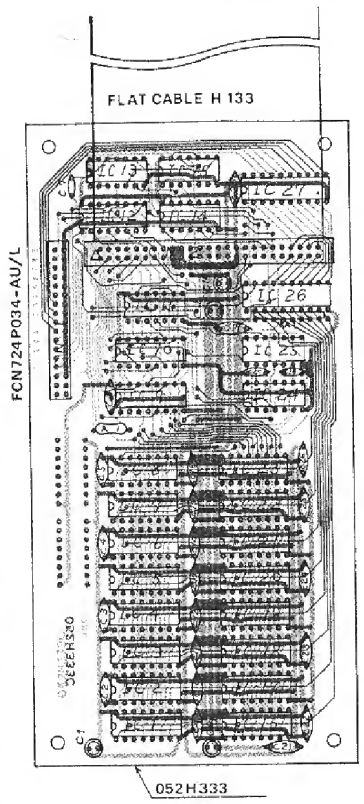
Trimmer SR19R
Polystyren
2SA1015-GR
2SC1923-O
2SC1815-GR
2SC2021 R or S
2SA1175 JF, HF, FF, EF, KF
or 2SA1115 E, F
(2SA937, early pcb)
060 Factory selected
Diode 1S2473
Jumper
Diode 1S1585
Zenner
FET NF510
LED
Polycarbonate pipe

KEY ASSY No. 2–No. 5
Switch KEH10903
KEY TOP KT3–1 BLUE or IVORY

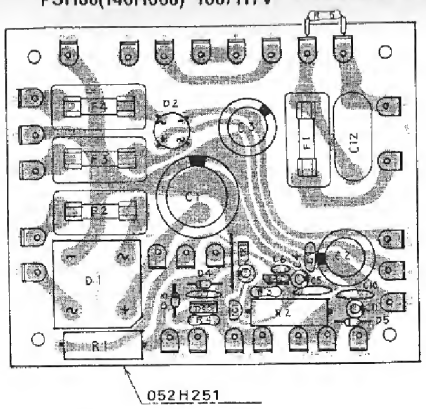


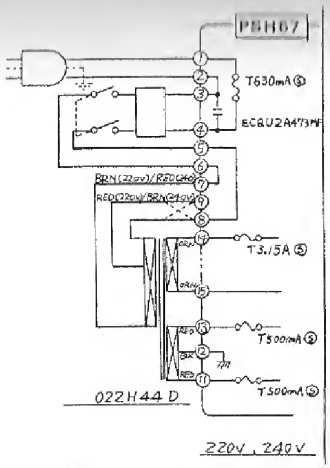

BUFFER
DATA BUS
RAM ADDRESS MPXs
LS00 ×¼
LS157
IC10
4116 × 8
IC16
IC17
IC18
IC19
IC20
IC21
IC22
IC23
IC26 LS245
LS157
IC9
IC1
IC2
IC3
IC4
IC5
IC6
IC7
IC8
RA1 4.7K×8
0.1 × 8
0.1 × 4
+5v
+12v
-5v
LS02 ×¾
LS04 ×⅙
IC14
IC12 LS368
IORQ CN2-38
IOPORT CN2-36
M1 CN2-40
RD CN2-39
WR CN2-37
Φ 4MHz CN2-35
RESET CN2-34
IC25 LS04 ×⅚
LS20
LS74
IC15
IC27 LS245
RAM BOARD
IC17,13,14,24,25
IC12

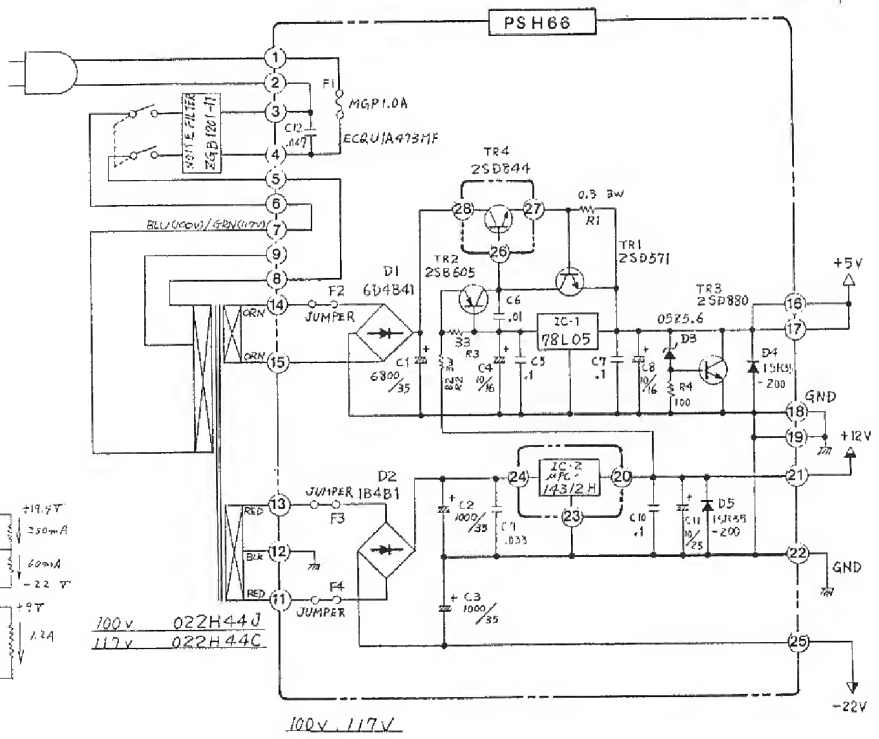
RAM BOARD OPH143(149H143)
(pcb 052H333C)



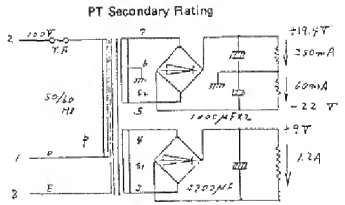
POWER SUPPLY BOARD
PSH67(146H067) 220/240V
PSH66(146H066) 100/117V (pcb 052H251A)



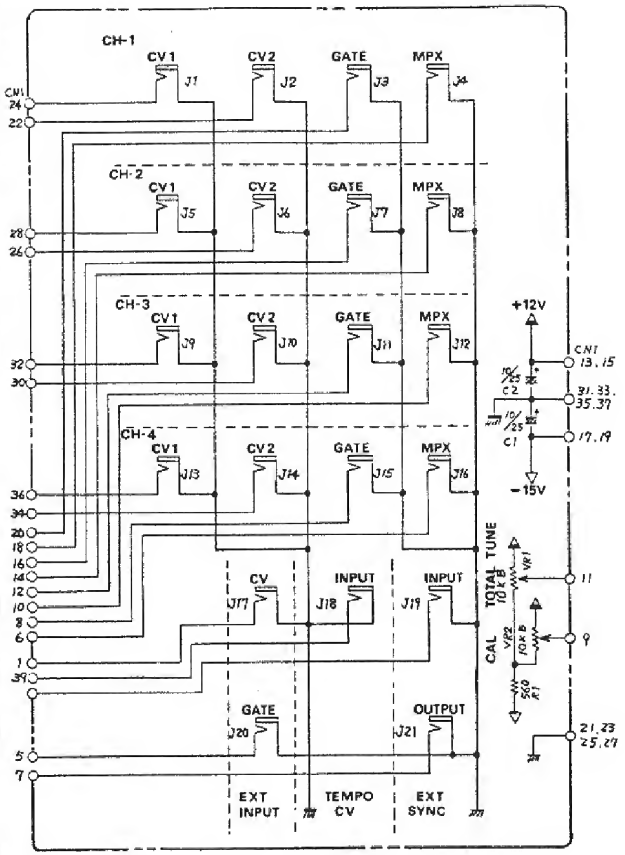


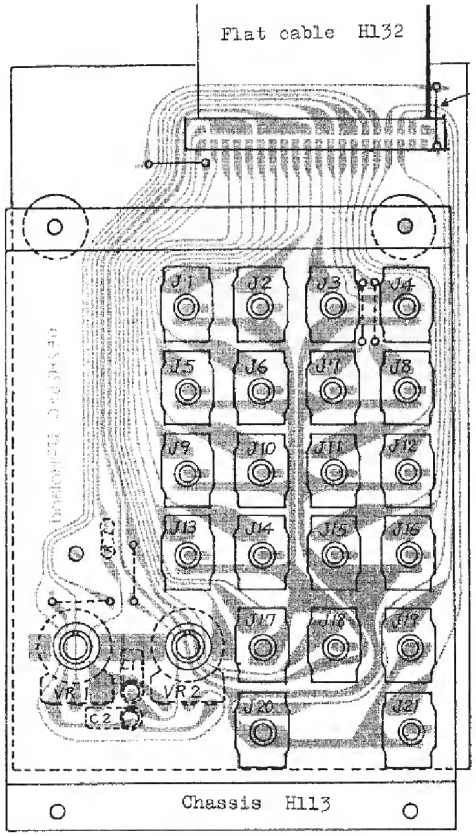


PT Secondary Rating

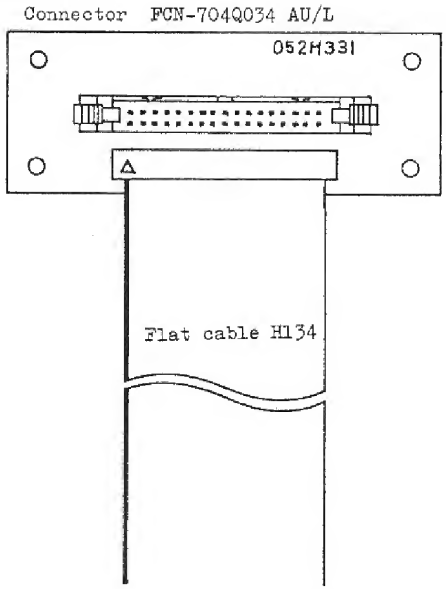


JACK BOARD
OPH142(149H142)
(pcb 052H285C)



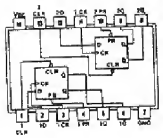


CONNECTOR BOARD
OPH144(149H144)
(pcb 052H331)



74LS74

Dual D-FFs with preset and clear

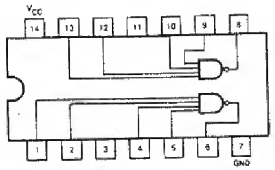


FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

74LS92

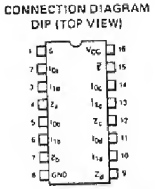
DUAL 4-INPUT NAND GATE



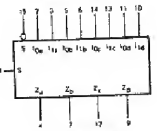
74LS157

QUAD 2-INPUT MULTIPLEXER

CONNECTION DIAGRAM DIP (TOP VIEW)



LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

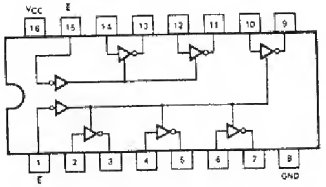
TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

74LS368

HEX 3-STATE INVERTER BUFFER
SEPARATE 2-BIT AND 4-BIT SECTIONS



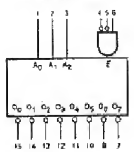
TRUTH TABLE

INPUTS		OUTPUT
$\overline{E}$	D	
L	L	H
L	H	L
H	X	(Z)

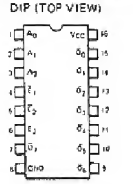
74LS138

1-OF-8 DECODER/DEMULTIPLEXER

LOGIC SYMBOL



CONNECTION DIAGRAM DIP (TOP VIEW)

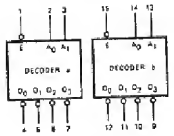


V_{CC} = Pin 16
GND = Pin 8

74LS139

DUAL 1-OF-4 DECODER

LOGIC SYMBOL



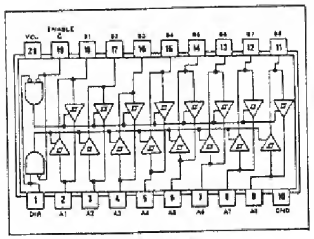
CONNECTION DIAGRAM DIP (TOP VIEW)

V_{CC} = Pin 16
GND = Pin 8

74LS245

Octal 3 State Bus Transceivers

(TOP VIEW)



FUNCTION TABLE

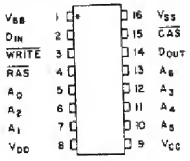
ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

MK4116

16,384 X 1-BIT DYNAMIC RAM

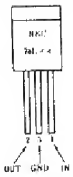
PIN CONNECTIONS



PIN NAMES

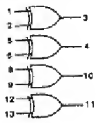
A_0-A_6	ADDRESS INPUTS	WRITE	READ/WRITE INPUT
CAS	COLUMN ADDRESS STROBE	V_{BB}	POWER (−5V)
		V_{CC}	POWER (+5V)
D_{IN}	DATA IN	V_{DD}	POWER (+12V)
D_{OUT}	DATA OUT	V_{SS}	GROUND
RAS	ROW ADDRESS STROBE		

μPC78L



MC14070B

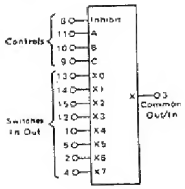
QUAD EXCLUSIVE "OR" GATE



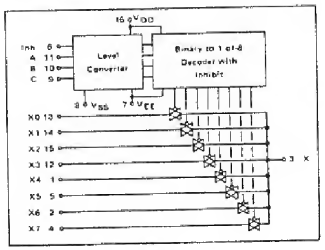
V_{DD} = Pin 14
V_{SS} = Pin 7
(Both Devices)

MC14051B

8-Channel Analog Multiplexer/Demultiplexer



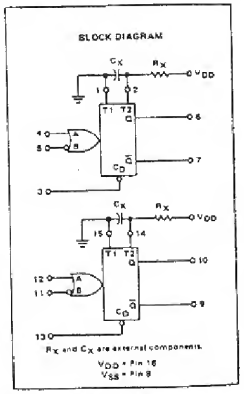
V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7



MC14528B

DUAL MONOSTABLE MULTIVIBRATOR

BLOCK DIAGRAM



TRUTH TABLE

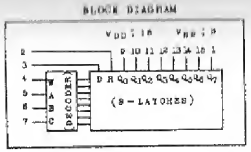
Write Disable	Reset	Addressed Latch	Unaddressed Latch
0	0	Data	Q_n*
0	1	Data	Reset†
1	0	Q_n*	Q_n*
1	1	Reset	Reset

* Q_n is previous state of latch.
† Reset to zero state.

TC4099BP

8-Bit Addressable Latch

BLOCK DIAGRAM



CONTROL INPUTS		ADDRESS INPUTS			OUTPUTS							
RESET	W/DIS	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
H	*	*	*	*	L	L	L	L	L	L	L	L
L	H	*	*	*	—	—	—	—	—	—	—	—
H	L	L	L	L	D	L	L	L	L	L	L	L
H	L	L	L	H	L	D	L	L	L	L	L	L
H	L	L	H	L	L	L	D	L	L	L	L	L
H	L	L	H	H	L	L	L	D	L	L	L	L
H	L	H	L	L	L	L	L	L	D	L	L	L
H	L	H	L	H	L	L	L	L	L	D	L	L
H	L	H	H	L	L	L	L	L	L	L	D	L
H	L	H	H	H	L	L	L	L	L	L	L	D
L	L	L	L	L	D	—	—	—	—	—	—	—
L	L	L	L	H	—	D	—	—	—	—	—	—
L	L	L	H	L	—	—	D	—	—	—	—	—
L	L	L	H	H	—	—	—	D	—	—	—	—
L	L	H	L	L	—	—	—	—	D	—	—	—
L	L	H	L	H	—	—	—	—	—	D	—	—
L	L	H	H	L	—	—	—	—	—	—	D	—
L	L	H	H	H	—	—	—	—	—	—	—	D

* ; DON'T CARE D ; DATA INPUT
— ; HOLDS PREVIOUS DATA

MC14518B

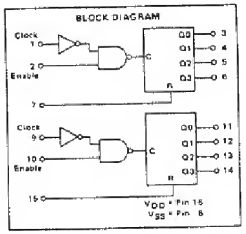
DUAL BCD UP COUNTER

TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
↑	1	0	Increment Counter
0	↓	0	Increment Counter
X	X	0	No Change
X	↓	0	No Change
↑	0	0	No Change
↓	X	0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don't Care

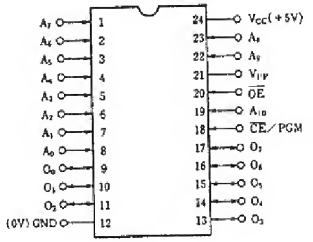
BLOCK DIAGRAM



μPD2716D

16K (2K × 8) UV ERASABLE PROM

(Top View)



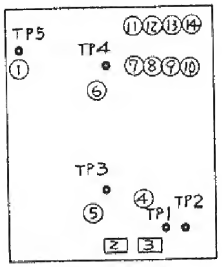
ADJUSTMENT

CPU BOARD

1 −15V

1-1 Connect digital voltmeter (DVM) across TP5 and TP2 (GND).

1-2 Adjust VR1 for -15.000±3mV.

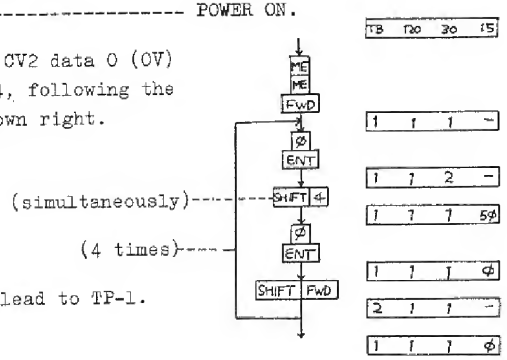


2 D/A OFFSET

2-1 Set controls:
TOTAL TUNE - center
CYCLE - OFF
SYNC - INT

2-2 ---------- POWER ON.

2-3 Write CV1 and CV2 data 0 (0V) for CH1 to CH4, following the flow chart shown right.



2-4 Shift the DVM lead to TP-1.

2-5 ---------- Flip MODE switch for PLAY mode.

2-6 ---------- Push ENTER. --------

2-7 Adjust VR4 for 0.000V. (0.000 to 0.099V)

Keep the CV data for the next adjustment.

3 CV OFFSET

This adjustment follows the preceding.

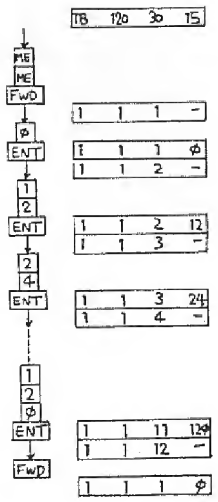
3-1 Insert plug with DVM into a CV jack.

3-2 Adjust related VR for 0.000V (0 to +0.2mV).

3-2 Repeat the step for the remainder.

CH-	4	3	2	1	
CV2	11	12	13	14	VR
CV1	7	8	9	10	

4 D/A, WIDTH



4-1 Turn power off then on.

4-2 Connect DVM to CH-1 CV1 jack.

4-3 Enter the CV data 0-120 in 12 increments.

4-4 Hereafter, pushing FWD button will change data (and CH-1 CV1 at the jack) and display by 12 at every step as shown below. Note that the data displayed on indicator lamp preceds actual data by one step.

Data displayed	Actual data	CV1 (To be ±1mV) volt
12	0	0.000
24	12	1.000
36	24	2.000
48	36	3.000
60	48	4.000
72	60	5.000
84	72	6.000
96	84	7.000
108	96	8.000
120	108	9.000
...	120	10.000
(0	120	10.000)

4-5 Adjust VR2 to the table above.
Use VR3 to compensate for higher CV only (data 72 and above).

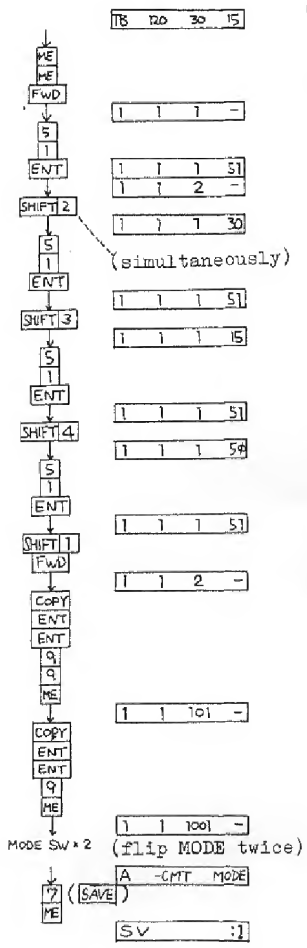
5 CMT FREQ

5-1 Flip MODE for PLAY.

5-2 With frequency counter connected to TP-4 adjust VR6 for 1.3kHz±5%.

5-3 Verfy that frequency changes to 2.1kHz ±5% when mode is set to CMT.

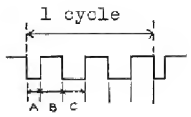
6 PLL FREQ



6-1 Connect CMT/SYNC IN and OUT with a cord.

6-2 Connect scope to TP-3.

6-3 Input data by following the chart shown at the left.
Waveform will appear on the screen.



A:B = 1:2

B:C = 1:1

6-4 Adjust VR5 for 50 duty ratio except A portion.

When waveform disappears during adjustment, push [7] and [ME] . In a few seconds waveform will reappear.

1 CMT CV REF

CAUTION

If trimmer wiper is frozen, try adjusting at component side.

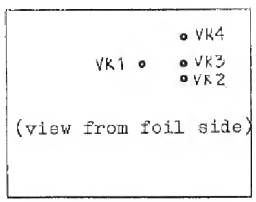
PAINT LOCKED !

1-1 et controls: TOTAL TUNE - center
TEMPO - center

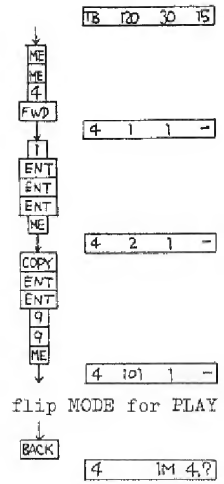
1-2 Connect CH-4 CV2 and TEMPO CV IN jacks with a cord.

1-3 Input data as shown right.

1-4 While plugging out and in the cord at TEMPO CV IN jack, adjust VR4 so that "time" being displayed remains unchanged.



CONTROL BOARD



2 CMT FREQ, LINEAR, OFFSET

2-1 Observe steps 1-1 and 1-2 above.

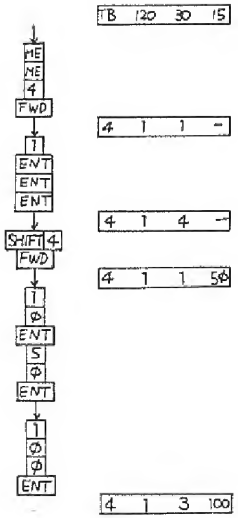
2-2 Enter data as illustrated at right.

2-3 Connect frequency counter to collector of TR28.

2-4 Adjust VRs respectively for the frequency in the table below.
To change data push FWD .
First, coarsely adjust VR3 for 100kHz, then the remainder.

2-5 Repeat adjustment until correct frequencies are obtained.

CV2	VR	Freq.
1Ø	VR2	20kHz
5Ø	VR3	100kHz
1ØØ	VR1	200kHz



PARTS LIST

CHASSIS

061H113	Chassis H113
061H112	Chassis H112
083H037	Side panel H37 (right)
083H038	Side panel H38 (left)
072H074	Panel H74
048H025	Heat sink H25
116H005	Joint screw H6
065H082	Cover H82 (fluorescent tube)
065H091	Cover H91 (rear cover)

KNOB

2247540600	K34 TYPE METAL

KEY TOP

12479704	KT3-2 blue (tandem)
12479705	KT3-1 ivory, blue

JACK

13449220	HLJ-102-01-010
1344940600	HSJ-779-01-010 (mini)

SLIDE SWITCH

13159113	SS8042-6LS

POWER SWITCH

13149103	2Wi XII

LEVER SWITCH

13139136	SLE-622-18P (CYCLE)
13139135	SLE-623-18P (SYNC)
13139132	SLE-722-18P (MODE)

KEY SWITCH

13129714	KEH10903 w/o key top
13129716	KEH4A006 (10 KEY ASS'Y)

PCB

149H140	CPU	BOARD OPH140 (pcb 052H249C)
149H141	CONTROL	BOARD OPH141 (pcb 052H250E)
149H142	JACK	BOARD OPH142 (pcb 052H285C)
149H143	RAM	BOARD OPH143 (pcb 052H333C)
149H144	CONNECTOR BOARD	OPH144 (pcb 052H331)
146H066	POWER SUPPLY BOARD	PSH66 (pcb 052H251A) 100/117V
146H067	POWER SUPPLY BOARD	PSH77 (pcb 052H251A) 220/240V

SEMICONDUCTOR

IC

15199116	μPC14312H (TA78012P)	3-PIN REGULATOR
15179111	μPD780-1 (LH-0080A)	8-BIT MICROPROCESSOR
15179306	MB8118N (M5K4116)	16,384 x 1-BIT DYNAMIC RAM
15179605BO	M5L2716K (MB8516)	16K (2K x 8) UV ERASABLE PROM
151791108O	M5L8253P-5 (μPD8253-5)	PROGRAMMABLE INTERVAL TIMER
15179120	LI2048	5 x 7 DOT MATRIX DECODER
15199109NO	μPC78L05 (TA78L005P)	3-PIN REGULATOR
15179128	μPD8255 (M5L8255AP)	PROGRAMMABLE PERIPHERAL INTERFACE
15169301HO	74LS00	QUAD 2-INPUT NAND
15169303HO	74LS02	QUAD 2-INPUT NOR
15169346BO	74LS03	HEX INVERTERS
15169304HO	74LS04	HEX INVERTERS
15169335HO	74LS20	DUAL 4-INPUT NAND
15169347BO	74LS32	QUAD 2-INPUT OR
15169311HO	74LS74	DUAL D-FFs WITH PRESET AND CLEAR
15169348BO	74LS132	QUAD 2-INPUT NAND SCHMITT TRIGGERS
15169318HO	74LS138	1-OF-8 DECODER/DEMULTIPLEXER
15169319HO	74LS139	DUAL 1-OF-4 DECODER
15169332HO	74LS157	QUAD 2-INPUT MULTIPLEXER
15169324CO	74LS245	OCTAL 3-STATE BUS TRANSCEIVERS
15169328HO	74LS368	HEX 3-STATE INVERTER BUFFER
15169117	7407	HEX O.C. BUFFERS
151891160A	TL080CP	OP AMP (factory selected)
15189117	TL081CP	OP AMP
15189118	TL082CP	OP AMP
15189111NO	μPC311C	OP AMP
15189105	μPC4558C	OP AMP
15219105	LM565	PHASE LOCKED LOOP
15159104TO	TC4011BP	QUADRUPLE 2-INPUT NAND GATE
15159112TO	TC4049BP	HEX BUFFER/CONVERTER (INVERTING)
15159113HO	TC4051BP	8-CHANNEL ANALOG MULTIPLEXER/DEMALTIPLEXER
15159117TO	TC4070BP	QUAD EXCLUSIVE "OR" GATE
15159120TO	TC4099BP	8-BIT ADDRESSABLE LATCH
15159309TO	TC4528BP	DUAL MONOSTABLE MULTIVIBRATOR

TRANSISTOR

15129816	2SD880-Y or O, GR
15129606	2SD844-Y
15129600	2SD571-L
15119402	2SA682-Y
15119123	2SA1175-JF or HF, FF, EF, KF, (2SA1115-E or F), (2SA937)
15119113	2SA1015-GR
15119601	2SB605-L
15129121	2SC2021-R or S
15129708	2SC1226-A
1512913200	2SC1923-O
15129114	2SC1815-GR
15139103	2SK30A-GR
15139110	NF510 or 2N4392

DIODE

15019247	GP-30G (Hi-Fi Special)
15019208	1SR35-200
15019123	1S1585
15019103	1S2473
15019624	1SZ52
15019631	05Z7.5-Y
15019632	05Z36-X
15019612	05Z5.1-X
15019628	05Z5.6-U
15029103	TLR124 (red)
15029105	TLG124A (grn)
15029133	TLY124 (yel)
15019250	DS5BN-M
15019243	1B481
15029708	16MD-02Z fluorescent lamp indicator

POTENTIOMETER

ROTARY

13219601	VM10R-S20A15 (100KA) TEMPO
13219312	EVH-LWAD25B14 (10KB)

TRIMMER

	SR19R
13299111	2.2KB
13299114	10KB
13299115	22KB
	RJ-6S
13299306	500Ω B
13299307	1KB
	RJ-6P
13299131	20KB

RESISTOR

	CRB25FX (1% +100ppm/°C)
13769152DO	1.3K
13769169DO	47K
13769197DO	100K
13769201DO	150K
	CRB25DZ (0.5% +25ppm/°C)
13789601DO	100K
13789602DO	130K
	CRB25BY (0.1% +50ppm/°C)
13789501DO	11K
13789507DO	31K
13789503DO	125K
13789504DO	250K
	CRB25DY (0.5% +50ppm/°C)
13789113DO	500K
13789114DO	1M
	ARRAY
13919108	4R7K x 4 (RGSD4 x 472K)
13919109	4R7K x 8 (RGSD8 x 472K)
13919110	22K x 8 (RGSD8 x 223K)
	MO-4S
13839143F0	0.33Ω 3W
13839145F0	82Ω 3W

CAPACITOR

13569153	CQ09S-1H-22000-J05	2200P 50V J (polystyrene)
13569152	CQ09S-1H-240RO	240P 50V J (polystyrene)
13569151	CQ09S-1H-022RO	22P 50V J (polystyrene)

CONVERTER TRANSFORMER

12449105	S167724

POWER TRANSFORMER

022H044J	100V
022H044C	117V
022H044D	220/240V

NOISE FILTER

12449219	ZGB1201-11 (100/117V)
12449220	ZMB2201-13 (220/240V)

FUSE

12559133	MGP1.0A	PRIM. 100/117V
12559532	CEE T630mA	PRIM. 220/240V
12559518	CEE T500mA	SEC. 220/240V
12559516	CEE T3.15A	SEC. 220/240V

SPEAKER

12389806	EAF-16R02C

FLAT CABLE

053H131	FLAT CABLE H131
053H132	FLAT CABLE H132
053H133	FLAT CABLE H133
053H134	FLAT CABLE H134

IC SOCKET

13429511	IC-49-2406#2 (24P)

CONNECTOR

13429608	TCSC 250-1-1
13439178	FCN-704Q034-AU/L 34PIN
13429179	FCN-724P034-AU/L 34PIN
13439176	FCN-724P040-AU/L 40PIN
13439177	FCN-724P050-AU/L 50PIN
13439120	5045-04A
13439121	5045-05A
13439122	5045-06A
13439126	5045-10A

OTHERS

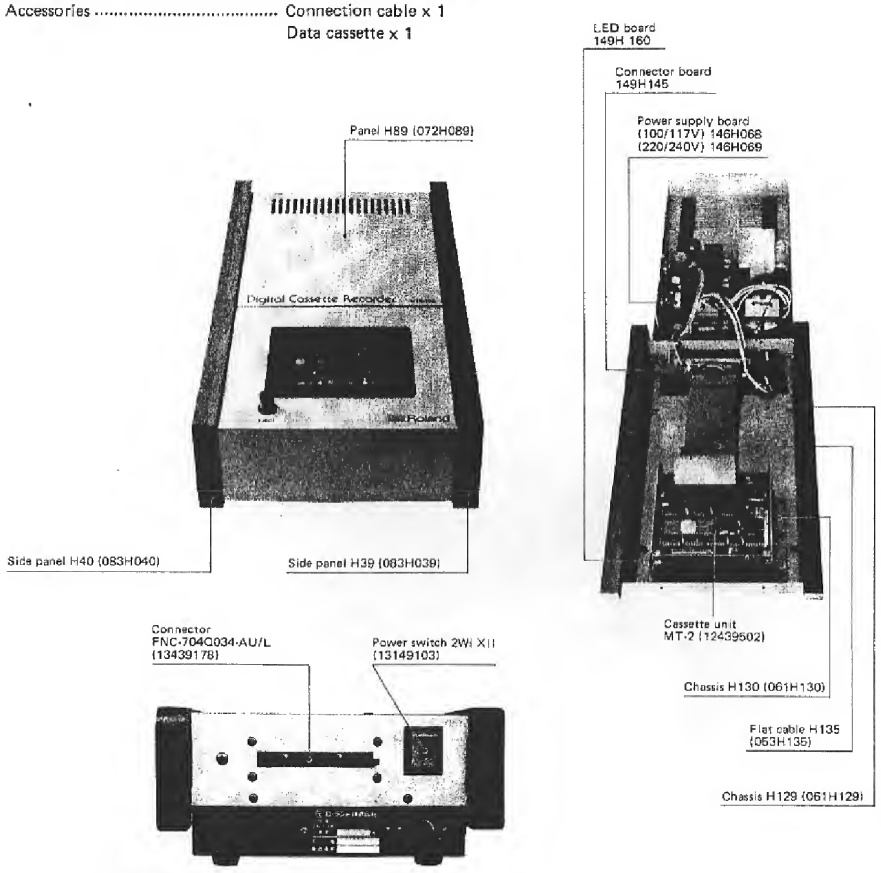
2215050100	LONG NUT #1
2215050300	LONG NUT #3
065H090	Cover H90 (radiation cover)
065H190	Cover H190 (lever SW)
064H055	Holder H55 (pot.)
064H083	Holder H83 (key SW assy 4)
064H092	Holder H92 (key SW assy 1, 2, 3)
064H111	Holder H111 (key SW assy 5)
107H061	Cushion H61

MTR-100 SERVICE NOTES

First Edition

SPECIFICATIONS

Memory Capacity	250 K bytes (Each side of a tape)
Dimensions	218 x 348 x 118 mm
Weight	3.4 Kg
Power	25 W (Dom), 30 W (Exp)
Accessories	Connection cable x 1
	Data cassette x 1



PARTS LIST

CHASSIS

061H129	Chassis H129 (MAIN)
061H130	Chassis H130

PANEL

072H089	PANEL H89
107H062	Cushion H62
048H026	Heat sink H26
083H039	Side panel (right) H39
083H040	Side panel (left) H40

FLAT CABLE

053H135	Flat cable H135
053H136	Flat cable H136

CASSETTE UNIT

12439502	MT-2

POWER SWITCH

13149103	2Wi XII

PCB

146H068	Power supply board PSH68 100/117V (pcb 052H334)
146H069	Power supply board PSH69 220/240V (pcb 052H334)
149H160	LED board OPH160 (pcb 052H336)
149H145	Connector board (pcb 052H331)

SEMICONDUCTOR

IC

15199101F0	μA723DC

TRANSISTOR

15129114	2SC1815-GR
15129825	2SD844-O

DIODE

15029103	TLR124 (LED)
15019103	1S2473
15019250	DS5BN-M
15019634	RD3.9EB

POTENTIOMETER

TRIMMER

13299109	1KB (SR19R)

RESISTOR

	MO-4S
13839146F0	4.0Ω (3W)
13839147F0	1.5Ω (3W)

CONNECTOR

13439178	FCN-704Q034-AU/L 34 pin
13439123	5045-07A
13439180	5273-07A

POWER TRANSFORMER

022H046J	PTH-046J	100V
022H046C	PTH-046C	117V 3P CSA
022H046D	PTH-046D	220V, 240V

FUSE

12559133	MGP1.0A
12559532	CEE T630mA
12559514	CEE T2.0A
12559516	CEE T3.15A

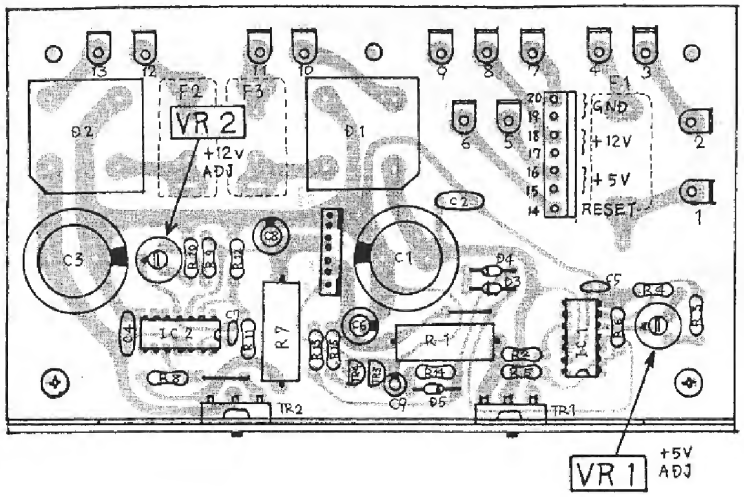
NOISE FILTER

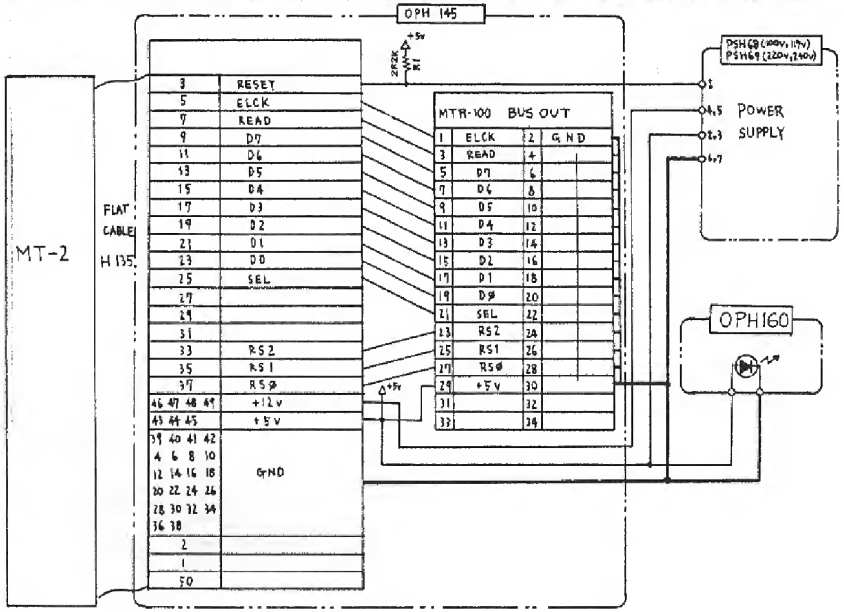
12449219	ZGB1201-11 (100/117V)
12449220	ZMB2201-13 (220/240V)

OTHERS

2215050300	Long nut #3 (18mm)
2215050100	Long nut #1 (10mm)

POWER SUPPLY BOARD
PSH68(146H068) 100/117V/PSH69(146H069) 220/240V
(pcb 052H334)

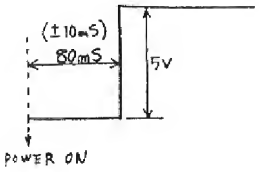




ADJUSTMENT

Measurements must be done without disconnecting connector housing.

1. Adjust VR1 for + 5.00V.
2. Adjust VR2 for + 12.00V.
3. Confirm RESET Signal at Pin 14 upon power ON.



NOTE: MT-2 is, as a whole, named maker-only-repairable component.
The Roland Company will promptly supply the replacement or repair the unit upon reception.
Please do not disassemble the unit in question as this will void the service polycy.
Return complete MT-2 with a tag identifying the unit by using the model version and serial number of the MTR-100 in which it is used.